IN THE CLAIMS

Please add new claims 21-31 as follows:

1-12 (Cancelled)

13. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device including a memory cell constituted by a MISFET and a capacitor, comprising steps of:

forming the MISFET on a semiconductor substrate;

forming an insulating film on said MISFET;

depositing a first shielding film on said insulating film;

depositing, on an upper surface of said first shielding film,

a first conductive film, a capacitive insulating film comprised of a high-dielectric-constant material, and a second conductive film; patterning said second conductive film and said capacitive insulating film exclusive of said first shielding film; and thereby forming, on said first

shielding film, a capacitor constituted by a lower electrode comprised of said first conductive film, said capacitive insulating film, and an upper electrode comprised of said second conductive film; and

forming a second shielding film covering sidewalls of said upper electrode and said capacitor and being comprised of an insulating film contacting with an upper surface of said first shielding film,

wherein said capacitor is disposed on said MISFET through said insulating film,

said capacitor is covered with said first and second shielding films,

a plug is formed so that a conductive film is embedded into a first contact hole formed by removing said insulating film and said first shielding film on a source or drain region of said MISFET, said plug being connected to said lower electrode,

a second contact hole is formed in said insulating film disposed on the other of the source or drain region of said MISFET, and

the other of the source or drain region of said MISFET is connected through said second contact hole to a wiring formed on an upper portion of said insulating film.

14. (Previously Presented) The method of manufacturing a semiconductor integrated circuit device according to claim 13,

wherein said first shielding film is formed so as to cover a forming region of said MISFET, and

said second contact hole is formed in said first shielding film.

15. (Previously Presented) The method of manufacturing a semiconductor integrated circuit device according to claim 14,

wherein said second shielding film is formed so as to cover a formation region of said MISFET, and

said second contact hole is formed in said second shielding film.

16. (Previously Presented) The method of manufacturing a semiconductor integrated circuit device according to claim 14, wherein said first shielding film is comprised of an insulating film.

17. (Previously Presented) The method of manufacturing a semiconductor integrated circuit device according to claim 13, wherein said step of forming the insulating film includes a step of annealing in a hydrogen atmosphere.

18. (Previously Presented) A method of manufacturing a semiconductor integrated circuit device including a memory constituted by a MISFET and a capacitor, comprising steps of:

forming a MISFET on a semiconductor device;

forming an insulating film on said MISFET;

depositing a first shielding film on said insulating film;

depositing a first conductive film, a capacitive insulating film comprised of a ferroelectric material, and a second conductive film on said first shielding film; patterning said second conductive film and said capacitive insulating film exclusive of said first shielding film; and thereby forming, on said first shielding film, a capacitor constituted by a lower electrode comprised of said first conductive film, said capacitive insulating film, and an upper electrode comprised of the second conductive film; and

forming a second shielding film comprised of an insulating film so as to cover sidewalls of said upper electrode and said capacitor and contact with said first shielding film,

wherein said capacitor is disposed on said MISFET through said insulating film,

said capacitor is covered with said first and second shielding films,

said first shielding film is formed so as to cover a formation MISFET forming region,

a plug is formed so that a conductive film is embedded in a first contact hole formed by removing said insulating film and said first shielding film disposed on a source or drain region of said MISFET, said plug being connected to said lower electrode,

a second contact hole is formed in said insulating film disposed on the other of the source or drain region of said MISFET, and

the other of the source or drain region of said MISFET is connected to a wiring through said second contact hole.

19. (Previously Presented) The method of manufacturing a semiconductor integrated circuit device according to claim 18,

wherein said second shielding film is formed so as to cover the said MISFET forming region,

said second contact hole is formed in said second shielding film, and

said first shielding film is comprised of an insulating film.

20. (Previously Presented) The method of manufacturing a semiconductor integrated circuit device according to claim 18, wherein said wiring is formed on an upper portion of said insulating film.

21. (New) A semiconductor integrated circuit device comprising:

(a) an information transfer MISFET including a gate insulating film formed over a semiconductor substrate, a gate electrode formed over the gate insulating film, and source and drain regions formed in the semiconductor substrate on both sides of said gate electrode;

(b) an insulating film formed over said information transfer MISFET;

(c) a capacitor including a lower electrode comprised of a first conductive film, a capacitive insulating film formed over said lower electrode and comprised of a high-dielectric or ferrodielectric material, and a lower electrode comprised of a second conductive film and electrically connected to one of said source and drain regions; and

(d) a first shielding film comprised of an insulating film formed under said lower electrode and a second shielding film comprised of an insulating film formed on said upper electrode,

wherein said capacitor is covered with said first and second shielding films,

said capacitor is formed over said source or drain region of said information transfer MISFET through said insulating film,

said first shielding film and second shielding film are formed over said source and drain regions of said information transfer MISFET, and

a plug is formed in a contact hole formed by removing said insulating film and said first shielding film located on another of said source and drain regions of said information transfer MISFET, with a conductive film being embedded in the plug, and is connected to said lower electrode.

22. (New) The semiconductor integrated circuit device according to claim 21,

wherein said first shielding film is formed by a pattern larger than that of said lower electrode, and

said second shielding film is formed so as to cover an upper surface and a sidewall of said upper electrode, a sidewall of said capacitive insulating film, and a sidewall of said lower electrode by being connected to said first shielding film outside said lower electrode.

23. (New) A semiconductor integrated circuit device comprising:

(a) an information transfer MISFET including a gate insulating film formed over a semiconductor substrate, a gate electrode formed over the gate insulating film, and source and drain regions formed in the semiconductor substrate on both sides of said gate electrode;

(b) an insulating film formed over said information transfer MISFET;

(c) a capacitor including a lower electrode comprised of a first conductive film formed over said insulating film, a capacitive insulating film formed over said lower electrode and comprised of a high-dielectric or ferrodielectric material, and an upper electrode comprised of a second conductive film; and

(d) a shielding film formed so as to cover a sidewall of said lower electrode and an upper portion and a sidewall of said upper electrode,

wherein said shielding film includes a second shielding film formed by a pattern larger than that of said lower electrode and covering the upper portion and sidewall of said upper electrode, and a first shielding film formed under said second shielding film and formed so as to overlap with said second shielding film outside said lower electrode,

said first and second shielding films are each comprised of an insulating film,

said capacitor is formed over said source or drain region of said information transfer MISFET through said insulating film,

said first shielding film and said second shielding film are formed on said source and drain regions of said information transfer MISFET,

a plug is formed in a first contact hole formed by removing said insulating film and said second shielding film located on one of said source and drain regions of said information transfer MISFET, with a conductive film being embedded in the plug, and is connected to said lower electrode, and

a second contact hole is formed in said insulating film and said second shielding film located on another of said source and drain regions of said information transfer MISFET, and is connected to a wiring.

24. (New) The semiconductor integrated circuit device according to claim 21,

wherein said second shielding film is formed by a pattern larger that that of said lower electrode, and

said first shielding film is formed so as to overlap with said second shielding film outside said lower electrode.

25. (New) The semiconductor integrated circuit device according to claim 21,

wherein said first and second shielding films and said capacitive insulating film is insulating films each made of a lead compound, and

a lead composition ratio of each of said shielding films is set higher than that of said capacitive insulating film.

26. (New) The semiconductor integrated circuit device according to claim 21, wherein said capacitive insulating film is a first PZT film ($Pb_{x1}(Zr_{y1}Ti_{z1})O_3$), and

said first and second shielding films are second PZT films ($Pb_{x2}(Zr_{y2}Ti_{z2})O_3$)(X2 > X1).

27. (New) The semiconductor integrated circuit device according to claim 21,

wherein an interlayer insulating film having barrier layers on said information transfer MISFET and capacitor is formed, and

a wiring is formed on said interlayer insulating film.

28. (New) The semiconductor integrated circuit device according to claim 27, wherein said barrier layer is made of a lead compound or is a PZT film, Al_2O_3 film or amorphous film.

29. (New) The semiconductor integrated circuit device according to claim 27, further comprising: a contact hole formed in said interlayer insulating film, wherein bottom and side portions of said contact hole are covered with a TiN film.

30. (New) The semiconductor integrated circuit device according to claim 27, further comprising:

a plurality of wirings including said wiring; and

another interlayer insulating film having the same constitution as that of said interlayer insulating film formed between the wirings.

31. (New) The semiconductor integrated circuit device according to claim 27, further comprising: a passivation film formed on an uppermost layer of said plurality of wirings, wherein said passivation film having a barrier layer.